Phase I –Final Review

 APPLIED ELECTRONICS **Date:10.11.12**

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| **S.No** | **Reg.No** | **Name of the candidate** | **Title** | **NAME OF THE****SUPERVISOR** | **PPT****(50)** | **Demo****(50)** |
| 1 | 11711401001 | AARTHI KJ VERONICA | MEMS Gyroscope based Motion sickness estimation system | DR.T.SURESH | 45 |  |
| 2 | 11711401002 | M.BENNITO RAJ | An approach to Iris Recognition based on artificial bee colony algorithm | S. JOSHUA KUMARESAN | 46 |  |
| 3 | 11711401003 | A.BHARATHI PRIYA | MRI Brain Image Segmentation For Spotting Tumors | DR.D.EBENEZER/ G.BABU | AB |  |
| 4 | 11711401004 | V.GAUTHAM GOVINDH | A Novel Algorithm For Automatic Segmentation Of Lung Nodules | DR.R.SIVAKUMAR | 47 |  |
| 5 | 11711401005 | V.JAI CHANDRAN | Image Recognition And Processing Using ANN | G.BABU | AB |  |
| 6 | 11711401006 | K.KAVITHA | Segmentation of retinal vessels to determine arteriolar to venular ratio | DR.R.SIVAKUMAR | 43 |  |
| 7 | 11711401007 | A.LOGESWARI | Digital Signal Processing & Algorithm For Gamma Ray Tracking | DR.D.EBENEZER/ G.BABU | AB |  |
| 8 | 11711401008 | L.MUGILVANNAN | Low Power and Area Efficient Carry Select Adder | DR.S.RAMASAMY | 45 |  |
| 9 | 11711401009 | P.NAVION DHALIA | Reconfiguration Of Optical Network For Dynamic Traffic | DR.R.SIVAKUMAR | AB |  |
| 10 | 11711401010 | S.PRAVIN KUMAR | Human Authentication Based On Dental Biometrics | DR.R.SIVAKUMAR | 45 |  |
| 11 | 11711401011 | C. RATHINA KUMAR | Power Efficient Viterbi Decoder for Storage Devices | P.LATHA | 42 |  |
| 12 | 11711401012 | P.SANTHOSHINI | Automatic Segmentation of femur bone features and analysis of osteoporosis  | DR.R.SIVAKUMAR | 48 |  |
| 13 | 11711401013 | D.SATHISH KUMAR | Real Time Face Recognition Using optical flow algorithim & Histogram Equalization | S. JOSHUA KUMARESAN | 40 |  |
| 14 | 11711401014 | SHARON PREETHI.G | FPGA implementation and analysis of light weight scalable encryption algorithm | T.BLESSLIN SHEBA | 43 |  |
| 15 | 11711401015 | V.SHOBANA | Automated Data Logging Based On Low Cost Wireless Sensor Network | G.BABU | AB |  |
| 16 | 11711401016 | S.SHAYAMALA | Improved Architecture For A Floating Point Adder/Sub Unit | D.RUKMANI DEVI | AB |  |
| 17 | 11711401017 | T.SUJIN | Iris recognition based on cuckoo search algorithm | S. JOSHUA KUMARESAN | 44 |  |
| 18 | 11711401018 | E.R.TINTU | Improved video steganography using inter pixel value coding | T.BLESSLIN SHEBA | 42 |  |

VLSI DESIGN Date:09.11.12

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| **S.****No** | **Reg.No** | **Name of the candidate** | **Title** | **Name of the supervisor** | **PPT****(50)** | **Demo****(50)** |
| 1 | 111711419001 | ANJI SALAPAKSHI | ASIC Implementation Of Direct Digital Synthesizer | DR.S.RAMASAMY | Re do |  |
| 2 | 111711419002 | S.ARCHANA | Area efficient SAD architecture for block based video compression standards | D.RUKMANI DEVI | 43 |  |
| 3 | 111711419003 | M.BHAGYASREE | A novel error detection and data recovery architecture for video compression applications | DR.D.EBENEZER | 47 |  |
| 4 | 111711419004 | CHENGANI VINOD CHANDRA | Test generation for Bench mark circuits | DR.S.RAMASAMY | 47 |  |
| 5 | 111711419005 | G.DINESH | Dynamic Reconfigurable Image Registration On FPGA platforms | G.BABU | Re do |  |
| 6 | 111711419006 | R.MOHAN | A fast memory BIST algorithm With Fail Pattern Identification  | K.G.SHANTHI | 43 |  |
| 7 | 111711419007 | P.PRIYANKA | Real Time Smart Car Lock Security System Using Detection And Recognition | DR.T.SURESH | AB |  |
| 8 | 111711419008 | P.LAVA KUMAR | Adaptive Multi Carrier OFDM SAR Signal Processing | DR.T.SURESH | AB |  |
| 9 | 111711419009 | S.RENUKA | Iris recognition using PSO algorithm for human identification | S. JOSHUA KUMARESAN | 45 |  |
| 10 | 111711419010 | SAHANA.S | Design Of 2D Rank Order Filter For Real Time Noise Cancellation In Image And Video Processing Using FPGA | T.BLESSLIN SHEEBA | AB |  |
| 11 | 111711419011 | K.SANGEETHA | An Accelerometer Based Digital Pen With A Trajectory Recognition Algorithm For Hand Written Digit And Gesture Recognisation Algorithm | DR.D.DEVARAJU | AB |  |
| 12 | 111711419012 | SANJANA |  | D.RUKMANI DEVI | AB |  |
| 13 | 111711419013 | P.SARAVANAN |  Design and Implementation of FPGA based Direct Digital Frequency Synthesizer  | DR.S.RAMASAMY | 43 |  |
| 14 | 111711419014 | P.SUDHARSAN | Implementation and computational complexity evaluation of new switching based median filtering scheme for high density salt and pepper noise removal | DR.D.EBENEZER | 42 |  |
| 15 | 111711419015 | VELKUMAR G N | An advanced device and host SATA IP core with high speed transfer and error control | DR.D.EBENEZER | 46 |  |
| 16 | 111711419016 | RAVIKIRAN | A Network On Chip Architecture for optimization of area and power With Reconfigurable Topology on FPGAs | DR.D.DEVARAJU | 40 |  |
| 17 | 111711419017 | S.VINOTH RAJASINGH | Hardware Efficient Implementation Of adaptive filter Using Distributed Arithmetic  | K.G.SHANTHI | 42 |  |